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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/687,011	10/12/2000	JON SAUL	EMB1P004	1377

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C Douglas McDonald
Carlton Fields
PO box 3239
tampa, FL 33601-3239

EXAMINER	
BRODA, SAMUEL	

ART UNIT	PAPER NUMBER
2123	9

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/687,011	SAUL ET AL.	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 have been examined.

2. A review of the Application file indicates that an Information Disclosure Statement ("IDS") from another application was mistakenly entered into this Application as Paper No. 6. This IDS was removed and this Application no longer contains a paper named as "Paper No. 6." Applicants' own IDS mailed on 21 February 2001 was entered as Paper No. 7.

Drawings

3. The Draftsperson has objected to the drawings; see the copy of Form PTO-948 for an explanation.

Specification

3.1 The description portion of this Application contains a computer program listing consisting of more than three hundred (300) lines. In accordance with 37 CFR 1.96(c), a computer program listing printout of more than three hundred lines must be submitted as a computer program listing appendix on compact disc conforming to the standards set forth in 37 CFR 1.96(c)(2) and must be appropriately referenced in the specification (see 37 CFR 1.77(b)(4)). Accordingly, Applicants are required to cancel the computer program listing appearing in the specification on pages 58-71, file a computer program listing appendix on

compact disc in compliance with 37 CFR 1.96(c) and insert an appropriate reference to the newly added computer program listing appendix on compact disc at the beginning of the specification.

3.2 The incorporation of essential material in the specification by reference to a foreign application or patent, or to a publication is improper. Applicants are required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicant, or a practitioner representing the applicant, stating that the amendatory material consists of the same material incorporated by reference in the referencing application. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re Hawkins*, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

The attempt to incorporate subject matter into this Application by reference to the following:

(1) Jones at page 13;

(2) de Michelli at page 21;

(3) Goldberg at page 21;

(4) Madsen et al at page 23;

(5) Hoare at page 26; and

(6) Patterson et al page 27 (although Applicants do not explicitly invoke incorporation by reference),

is improper because this subject matter appears necessary to describe the claimed invention and provide an enabling disclosure of the claimed invention. See MPEP § 608.01(p).

3.3 The disclosure is objected to because the Specification at page 49 lines 15-16 contains the statement: "HTTP or other protocols could be readily substituted for HTML without undue experimentation." This statement appears to make no sense, because as stated by the Applicant at page 49 lines 20-21, "HTML is a simple data format used to create hypertext documents that are portable from one platform to another" whereas HTTP is a protocol used to transmit data.

Correction is required.

Claim Rejections - 35 U.S.C. § 112, First Paragraph

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.1 Claims 1-18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4.2 Regarding independent claim 1, this claim is directed at a "method for automatically partitioning a behavioral description" and includes the limitations:

(a) receiving a behavioral description of the electronic system;

(b) determining an optimal functionality between hardware and software of the electronic system; and

(c) partitioning implementation of the functionality between the hardware and software based on the determined optimal functionality.

As described below, the Specification appears to fail to describe how one or more of the claim limitations is accomplished.

Regarding the first step involving the behavioral description, the Specification at page 13 describes a "C-like description" including a "par" statement to describe process-level parallelism. According to the Specification at page 20 lines 14-21, this description is input to the parser 204 which creates an internal data structure called an "abstract syntax tree" that is sent to the partitioner 208. However, the Specification does not appear to describe: (1) how the "par" statement is parsed, or (2) the structure and contents of the "abstract syntax tree."

Regarding the second and third steps involving the determination of the optimal functionality and the partitioning, the Specification at page 21 lines 6-9 states that the partitioner 208 generates a control/data-flow graph from the abstract syntax tree, but the Specification does not appear to contain further description or flowcharts to describe this process.

Then according to the Specification at page 21 lines 9-13:

> . . . It then operates on the parts of the description which have not already been assigned to resources by the user. It groups parts of the description together into blocks, "partitioning blocks", which are indivisible by the partitioner. The size of these blocks is set by the user, and can be any size between a single operator, and a top-level process.

However, the Specification does not appear to contain further description or flowcharts to describe the method of grouping of parts of the description.

The Specification at page 21 then generally describes a genetic algorithm used to determine a candidate partition. According to the Specification at page 21 lines 18-23:

> . . . The algorithms all assign each partitioning block to one of the hardware resources which has been declared.
>
> The algorithms do this assignment so that the total estimated hardware area is smaller than the hardware resources available, and so that the estimated speed of the system is maximized.

The Specification at page 21 lines 28-29 states that "The resource on which each partitioning block is to be placed represents a gene . . ." and it is unclear from the quoted statements whether partitioning blocks are assigned to hardware resources, or hardware resources are assigned to partitioning blocks.

Additionally, other than the description of the "gene" and "fitness function" at pages 20-21, the Specification contains no further description or flowchart regarding how to program such a genetic algorithm. The genetic algorithm does not actually identify an optimal partition, but identifies an estimate of the optimal partition for a user-specified partition block size.

Finally, the Specification appears to provide little description regarding the system speed estimates made for hardware or software. For example, the Specification at page 23 lines1-4 describes hardware speed estimation as follows (emphasis added):

> . . . The speed and area of the resulting RTL level description is then estimated using **standard techniques**. For FPGAs the estimate of the speed is then decreased by a **non-linear factor** determined from the available free area, to take into account the slower speed of FPGA designs when the FPGA is nearly full.

The Specification does not appear to describe either any of the "standard techniques" or the "non-linear factor" that is used to perform the hardware speed estimation.

Taken as a whole, only with undue experimentation could one reasonably skilled in the art make and/or use the invention, because of the omissions in the subject matter described in the Specification.

4.3 Regarding independent claims 7 and 13, these claims are the corresponding computer program product and system claims of claim 1 and are rejected using the same analysis.

4.4 Dependent claims rejected but not described above are rejected based on their dependency to a rejected claim.

4.5 Claims 1-18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

4.6 Regarding independent claim 1, this claim is directed at a "method for automatically partitioning a behavioral description" and includes the limitation "determining an optimal functionality between hardware and software of the electronic system."

However, as described in Section 5.2 above, the genetic algorithm does not actually identify an optimal partition, but identifies an estimate of the optimal partition for a user-specified partition block size.

4.7 Regarding independent claims 7 and 13, these claims are the corresponding computer program product and system claims of claim 1 and are rejected using the same analysis.

4.8 Dependent claims rejected but not described above are rejected based on their dependency to a rejected claim.

Claim Rejections - 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> . . .
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.1 Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Srinivasan et al, "Hardware Software Partitioning with Integrated Hardware Design Space Exploration," IEEE Proceedings of Design, Automation, and Test in Europe, pp. 28-35 (February 1998).

5.2 Regarding claims 1 and 6, Srinivasan et al teaches a method for automatically partitioning a behavioral description of an electronic system between hardware and software for optimizing the system, including the steps of:

(a) receiving a behavioral description of the electronic system [tasks as part of discrete cosine transform input using behavioral language; see page 30 Fig. 3 and corresponding text];

(b) determining an optimal functionality between hardware and software of the electronic system [optimal functionality between hardware and software determined using a genetic algorithm that attempts to minimize a cost function; see pages 32-34]; and

(c) partitioning implementation of the functionality between the hardware and software based on the determined optimal functionality [partitioning determined by results of genetic algorithm; see pages 33-35, "Experimental Results"].

Therefore, Srinivasan et al anticipates claim 1.

5.3 Regarding claim 2, the method of Srinivasan includes implementation of functionality through varying parameters corresponding to chromosomes. See page 32 "4.2 GA for HW/SW Partitioning."

5.4 Regarding claim 3, the method of Srinivasan includes placing the hardware and software on a reconfigurable logic device. See page 30.

5.5 Regarding claim 4, the method of Srinivasan inherently includes output corresponding to processor description, machine code description, and hardware identification in order to partition the example algorithms shown in Tables 2 and 3 at pages 33-34.

5.6 Regarding claim 5, the cost function included in the method of Srinivasan hardware and software performance estimates for each of the different partitions. See pages 32-34.

5.7 Claims 7-12 are the computer program product claims corresponding to claims 1-6 and are rejected using the analysis of claims 1-6.

5.8 Claims 13-18 are the system claims corresponding to claims 1-6 and are rejected using the analysis of claims 1-6.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure. Reference to Wang et al, U.S. Patent 6,578,176, is cited as teaching method and system for genetic algorithm based power optimization.

Reference to Levi et al, U.S. Patent 6,539,532, is cited as teaching a method and apparatus for relocating elements in an evolvable configuration bitstream.

Reference to Govindarajan et al, "A Technique for Dynamic High-Level Exploration During Behavioral-Partitioning for Multi-Device Architectures," IEEE 13th International Conference on VLSI Design, pp. 212-219 (January 2000), is cited as teaching a partitioning-based exploration model.

Reference to Quan et al, "Preference-Driven Hierarchical Hardware/Software Partitioning," IEEE International Conference on Computer Design, pp. 652-657 (October 1999), is cited as teaching partitioning using a genetic algorithm that takes a hierarchical task graph as input.

Reference to Catania et al, "Applying Fuzzy Logic to Codesign Partitioning," IEEE Micro, pp. 62-70 (May/June 1997), is cited as teaching applying genetic algorithms to the partitioning process.

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (703) 305-1026. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER